Abstract of the Disclosure

A method for fabricating a non-volatile memory device is provided. The method for fabricating a non-volatile memory device includes the steps of: forming a gate pattern in which a first conductive layer is used as a floating gate, a second conductive layer is used as a control gate, the first conductive layer, a dielectric layer, and the second conductive layer are sequentially stacked on a semiconductor substrate; forming a polishing stopper on the gate pattern and the semiconductor substrate; forming an interlayer insulating layer on the polishing stopper; forming a common source line (CSL) by etching a portion of the interlayer insulating layer, and a portion of the polishing stopper, and depositing a conductive material to the etched portions; planarizing the common source line and the interlayer insulating layer until the surface of the polishing stopper is exposed; partially etching back the polishing stopper until the surface of the second conductive layer is exposed; and forming a silicide layer on the exposed second conductive layer and the common source line.